

SERVICE MANUAL

1750/1764

RAMERWEITERUNG FÜR C64 + C128
ENGLISCH

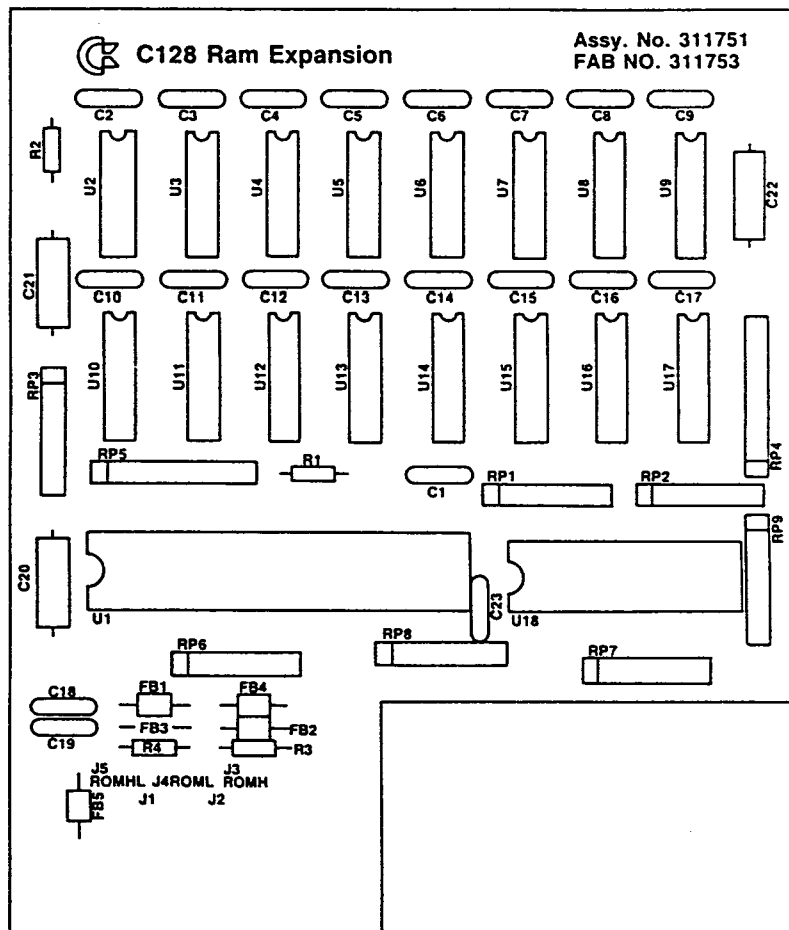
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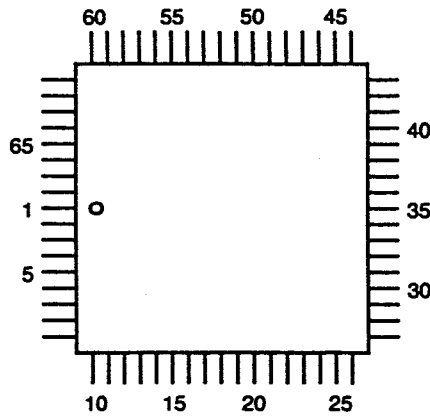
/RESET	1	64	VCC
/IRQ	2	63	BS
DOTCLK	3	62	CAS1
R/W	4	61	CAS0
1MHz	5	60	RAS1
/CS	6	59	RAS0
/BA	7	58	/DWE
/DMA	8	57	DD0
D7	9	56	DD1
D6	10	55	DD2
D5	11	54	DD3
D4	12	53	DD4
D3	13	52	DD5
D2	14	51	DD6
D1	15	50	DD7
D0	16	49	VSS
VSS	17	48	MA8
A15	18	47	MA7
A14	19	46	MA6
A13	20	45	MA5
A12	21	44	MA4
A11	22	43	MA3
A10	23	42	MA2
A9	24	41	MA1
A8	25	40	MA0
A7	26	39	TEST
A6	27	38	VSS
A5	28	37	VCC
A4	29	36	/ROMSEL
A3	30	35	/ROML
A2	31	34	/ROMH
A1	32	33	AO



A15-A0	These lines are bidirectional and buffered. They are used by the 8726 to access C128 memory and to detect address FF00. A0-A4 are used by the host processor to select the internal registers.	/IRQ	Output, active low. This line will go low if interrupts are enabled and any of the interrupt conditions have occurred.
D7-DO	Data lines used by the controller to output or input data from C128 memory. These lines are bidirectional and buffered. The host also uses these lines to access control registers.	MA8-MA0	Multiplexed address bus output to DRAMs. Includes full 256K addressing for use with 256K x 1 DRAMs.
R/W	This line is also bidirectional and buffered. It is used by the 8726 to perform either a read or write operation on system memory. The host uses this line to read or write to the controller registers. In both cases, a low on this line signifies a write operation and a high signifies a read.	DD0-DD7	Bidirectional data lines used by the controller to access expansion memory.
1Mhz	This input is the system clock and is used to synchronize all data transfers.	/DWE	Output, active low. When low, this line signifies that the controller is writing to expansion memory. This line is high during a read cycle.
/DMA	Output, active low. This signal is used by the 8726 to take control of the system buses prior to initiating a transfer sequence.	/RAS0	Output, active low. This line is used by the controller to access or refresh RAM BANK 0.
/BA	Input, active low. The 8726 monitors this signal to determine whether or not it can use the bus. On the C128, VIC generates this signal.	/RAS1	Output, active low. This line has the same function as /RAS0 except that it controls RAM BANK 1.
DOT CLOCK	This input is used to derive DRAM control signals.	/CAS0	Output, active low. Column address strobe for expansion bank 0.
/CS	Input, active low. This signal selects the 8726. This line must be brought low in order to access any of the internal registers.	/CAS1	Output, active low. Column address strobe for expansion bank 1.
RESET	Input, active low. A low on this line disables the controller and resets all internal registers. DRAM refresh is not interrupted during a reset.	BS	Bank Select. This input allows configuration of the controller for either of the two DRAM combinations.
		/ROMH	Input, active low.
		/ROML	Input, active low.
		/ROMSEL	Output, active low. This output is equal to the anding of /ROMH and /ROML.
		TEST	This input is for test purposes and has an internal pullup so that it may be left unconnected during normal operation.
		VCC	+5 volt supply.
		VSS	Ground.

315089-02

8726 QUAD - PACK VERSION



pin 1 — /RESET	pin 18 — VSS	pin 35 — /ROMH	pin 52 — VSS
pin 2 — /IRQ	pin 19 — A15	pin 36 — /ROML	pin 53 — DD7
pin 3 — DOTCLK	pin 20 — A14	pin 37 — /ROMSEL	pin 54 — DD6
pin 4 — R/W	pin 21 — A13	pin 38 — VCC	pin 55 — DD5
pin 5 — 1MHZ	pin 22 — A12	pin 39 — VSS	pin 56 — DD4
pin 6 — /CS	pin 23 — A11	pin 40 — TEST	pin 57 — DD3
pin 7 — /BA	pin 24 — A10	pin 41 — N.C.	pin 58 — DD2
pin 8 — /DMA	pin 25 — A9	pin 42 — MA0	pin 59 — DD1
pin 9 — D7	pin 26 — A8	pin 43 — MA1	pin 60 — DD0
pin 10 — D6	pin 27 — A7	pin 44 — MA2	pin 61 — /DWE
pin 11 — D5	pin 28 — A6	pin 45 — MA3	pin 62 — /RAS0
pin 12 — D4	pin 29 — A5	pin 46 — MA4	pin 63 — /RAS1
pin 13 — D3	pin 30 — A4	pin 47 — MA5	pin 64 — /CAS0
pin 14 — D2	pin 31 — A3	pin 48 — MA6	pin 65 — /CAS1
pin 15 — D1	pin 32 — A2	pin 49 — MA7	pin 66 — BS
pin 16 — D0	pin 33 — A1	pin 50 — MA8	pin 67 — VCC
pin 17 — N.C.	pin 34 — A0	pin 51 — N.C.	pin 68 — N.C.

