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6545-1 CRT Controller (CRTC)

CONCEPT

The 6545-1 is a CRT Controller intended to provide capability for interfacing the 6500/6800 microprosessor families to CRT or TV-type raster scan displays. A unique feature is the inclusion of several modes of operation, so that the system designer can configure the system with a wide assortment of techniques.

FEATURES

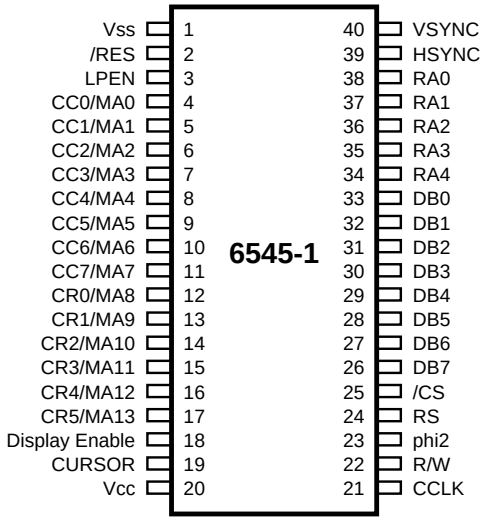
- Single +t volt (±5%) power supply.
- Alphanumeric and limited graphics capabilities.
- Fully programmable display (rows, columns, blanking, etc.).
- Non-interlaced scan.
- 50/60Hz operation.
- Fully programmable cursor.
- External light pen capability.
- Capable of addressing up to 16K character video display RAM.
- No DMA required.
- Pin-compatible with MC6845.
- Row/Column or straight-binary addressing for video display RAM.
- Internal 8-bit status register.

ORDERING INFORMATION

MXS 6545-1	1 MHz
MXS 6545A-1	2 MHz

PACKAGE DESIGNATOR
C = CERAMIC
P = PLASTIC

PIN DESIGNATION



MAXIMUM RATINGS

Supply Voltage, Vcc	-0.3V to +7.0V
Input/Output Voltage, Vin	-0.3V to +7.0v
Operating Temperature, Top	0˚C to 70˚C
Storage Temperature, Tstg	-55˚C to 150˚C

All inputs contain protection circuitry to prevent damage due to high static discharge. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

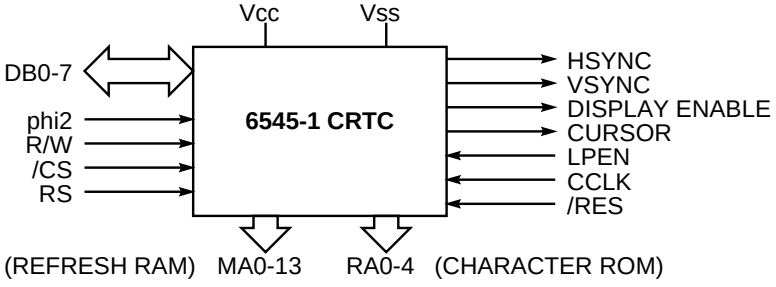
COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 5%, TA = 0-70˚C, unless otherwise noted)

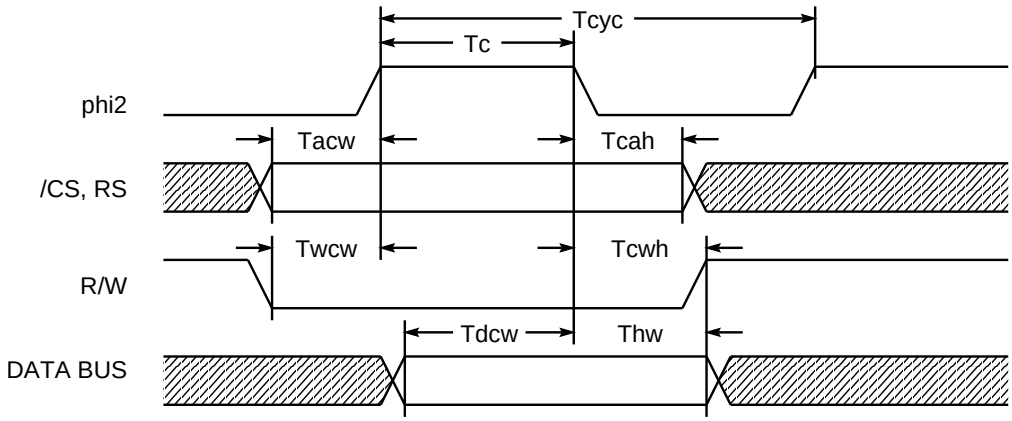
Symbol	Characteristic	Min.	Max.	Unit
Vih	Input High Voltage	2.0	Vcc	V
Vil	Input Low Voltage	-0.3	0.8	V
Iin	Input leakage current (phi2, R/W, /RES, /CS, RS, LPEN, CCLK)	-	2.5	µA
Itsi	Three-State Input leakage (DB0-7) Vin = 4V to 2.4V	-	10.0	µA
Voh	Output High Voltage Iload = 205µA (DB0-7) Iload = 100µA (all others)	2.4	Vcc	V
Vol	Output Low Voltage Iload = 1.6mA	Vss	0.4	V
Pd	Power Dissipation	-	1000	mW
Cin	Input Capacitance phi2, R/W, /RES, /CS, RS, LPEN, CCLK DB0-7	- -	10.0 12.5	pf pf
Cout	Output Capacitance	-	10.0	pf

INTERFACE DIAGRAM



MPU BUS INTERFACE CHARACTERISTICS

WRITE CYCLE



WRITE TIMING CHARACTERISTICS

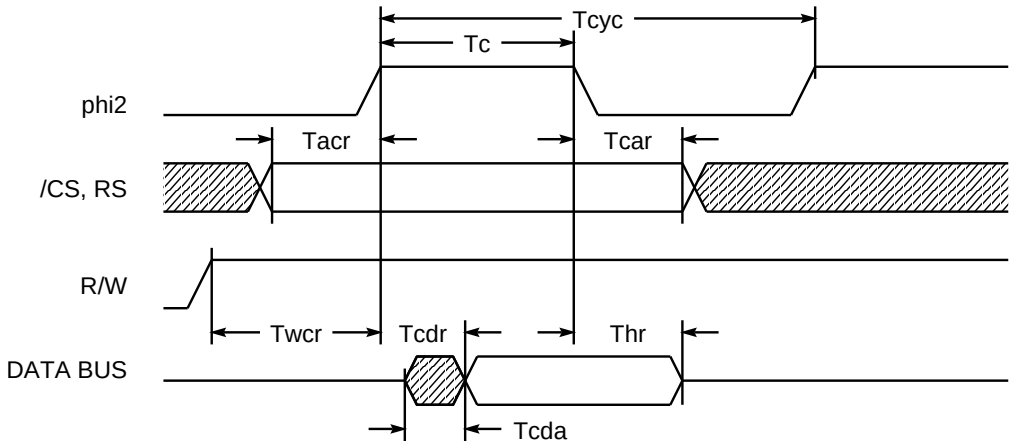
(Vcc = 5.0 ±5%, Ta = 0 to 70˚C, unless otherwise noted)

Symbol	Characteristic	6545-1		6545A-1		Unit
		Min.	Max.	Min.	Max.	
Tcyc	Cycle Time	1.0	40	0.5	40	µs
Tc	phi2 Pulse Width	470	-	235	-	ns
Tacw	Address Set-Up Time	180	-	90	-	ns
Tcah	Address Hold Time	0	-	0	-	ns
Twcw	R/W Set-Up Time	180	-	90	-	ns
Tcwh	R/W Hold Time	0	-	0	-	ns
Tdcw	Data Bus Set-Up Time	265	-	100	-	ns
Thw	Data Bus Hold Time	10	-	10	-	ns

(Tr and Tf = 10 to 30 ns)

MPU BUS INTERFACE CHARACTERISTICS

READ CYCLE



READ TIMING CHARACTERISTICS

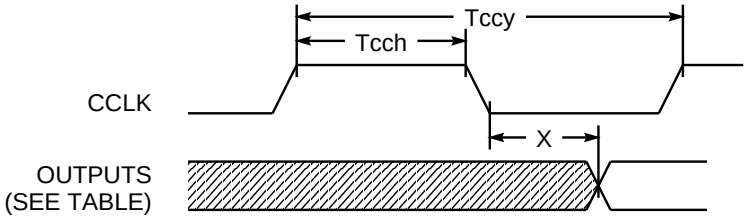
(Vcc = 5.0 ±5%, Ta = 0 to 70˚C, unless otherwise noted)

Symbol	Characteristic	6545-1		6545A-1		Unit
		Min.	Max.	Min.	Max.	
Tcyc	Cycle Time	1.0	40	0.5	40	µs
Tc	phi2 Pulse Width	470	-	235	-	ns
Tacr	Address Set-Up Time	180	-	90	-	ns
Tcar	Address Hold Time	0	-	0	-	ns
Twcr	R/W Set-Up Time	180	-	90	-	ns
Tcdr	Read Access Time	-	340	-	150	ns
Thr	Read Hold Time	10	-	10	-	ns
Tcda	Data Bus Active Time (Invalid Data)	40	-	40	-	ns

(Tr and Tf = 10 to 30 ns)

MEMORY AND VIDEO INTERFACE CHARACTERISTICS

(Vcc = 5.0 ±5%, Ta = 0 to 70˚C, unless otherwise noted)



SYSTEM TIMING

Output	Parameter
MA0-13	Tmad
RA0-4	Trad
Display-Enable	Tdtd
HSYNC	Thsd
VSYNC	Tvsd
CURSOR	Tcdd

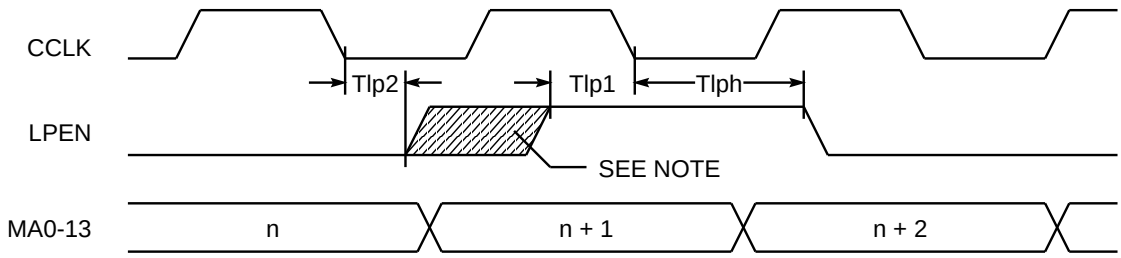
SYSTEM TIMING CHARACTERISTICS

(Vcc = 5.0 ±5%, Ta = 0 to 70˚C, unless otherwise noted)

Symbol	Characteristic	6545-1		6545A-1		Unit
		Min.	Max.	Min.	Max.	
Tccy	Character Clock Cycle Time	0.40	40	0.40	40	µs
Tcch	Character Clock Pulse Width	200	-	200	-	ns
Tmad	MA0-13 Propagation Delay	-	300	-	300	ns
Trad	RA0-4 Propagation Delay	-	300	-	300	ns
Tdtd	Display Enable Propagation Delay	-	375	-	375	ns
Thsd	HSYNC Propagation Delay	-	375	-	375	ns
Tvsd	VSYNC Propagation Delay	-	375	-	375	ns
Tcdd	CURSOR Propagation Delay	-	375	-	375	ns
Tlph	LPEN Hold Time	100	-	100	-	ns
Tlp1	LPEN Set-Up Time	20	-	20	-	ns
Tlp2	CCLK to LPEN Delay	0	-	0	-	ns

Ts, Tf = 20 ns (max)

LIGHT PEN STROBE TIMING DEFINITIONS



NOTE:"Safe" time position for LPEN positive edge to cause address n+2 to load into Light Pen Register. Tlp2 and Tlp1 are time positions causing uncertain results.

MPU INTERFACE SIGNAL DESCRIPTION

phi2 - (Clock)

The input clock is the system phi2 clock and is used to trigger all data transfers between the system microprosessor and the 6545-1.

R/W - (Read/Write)

The R/W signal is generated by the microprosessor and is used to control the direction of data transfer. A high on the R/W pin allows the prosessor to read the data supplied by the 6545-1; a low on the R/W pin allows a write to the 6545-1.

RS - (Register Select)

The Register Select input is used to access internal registers. A low on this pin permits writes into the Address Register and reads from Status Register. The contents of the Address Register is the identity of the register accessed when RS is high.

/CS - (Chip Select)

The Chip Select input is normally connected to the prosessor address bus either directly or through a decoder. The 6545-1 is selected when /CS is low.

DB0-7 - (Data Bus)

The DB0-7 pins are the eight data lines used for transfer of data between the prosessor and the 6545-1. These lines are bi-directional and are normally high-impedance except during read cycles when chip is selected.

VIDEO INTERFACE SIGNAL DESCRIPTION

HSYNC - (Horizontal Sync)

The HSYNC signal is an active-high output used to determine the horizontal position of displayed test. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC - (Vertical Sync)

The VSYNC signal is an active-high output used to determine the vertical position of displayed text. Like HSYNC, VSYNC may be used to drive CRT monitor or composite video generation circuits. VSYNC position and width are both fully programmable.

DISPLAY ENABLE

The DISPLAY ENABLE signal is an active-high output and is used to indicate when the 6545-1 is generating active display information. The number of horizontal displayed characters and the number of vertical displayed characters are both fully programmable and together are used to generate DISPLAY ENABLE signal. Display Enable can be delayed by one character time by setting bit 4 of R8 to a "1".

CURSOR

The CURSOR signal is an active-high output and is used to indicate when the scan coincodes with the programmed cursor position. The cursor position may be programmed to be any character in the address field. Furthermore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable. The CURSOR position may be delayed by one character time by setting bit 5 of R8 to a "1".

LPEN

The LPEN signal is an edge-sensitive input and is used to load the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active adge occurs. The active adge of LPEN is the low-to-high transition.

/RES - Reset Input

The /RES signal is an active-low input used to initialize all internal scan counter circuits. When /RES is low, all internal counters are stopped and cleared, all scan and video outputs are low, and control registers are unaffected. /RES must stay low for at least one CCLK period. All scan timing is initiated when /RES goes high. In this way, /RES can be used to synchronize display frame timing with line frequency.

MEMORY ADDRESS SIGNAL DESCRIPTION

MA0-13 - (Refresh RAM Address Lines)

These signals are active-high outputs and are used to address the Refresh RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of character/line and lines/frame.

There are two selectable address modes for MA0-13:

In the Straight Binary Mode, characters are stored in successive memory locations. Thus, the software must be designed so that row and column character co-ordinates are translated into sequentially-numbered addresses. In the Row/Column Mode MA0-7 become column addresses CC0-CC7 and MA8-13 become row addresses CR0-5. In this case, the software can manipulate characters in terms of row and column locations, but additional address compression circuits are needed to convert the CC0-7 and CR0-5 addresses into a memory efficient binary address scheme.

RA0-4 - (Raster Address Lines)

These signals are active-high outputs and are used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

DESCRIPTION OF INTERNAL REGISTERS

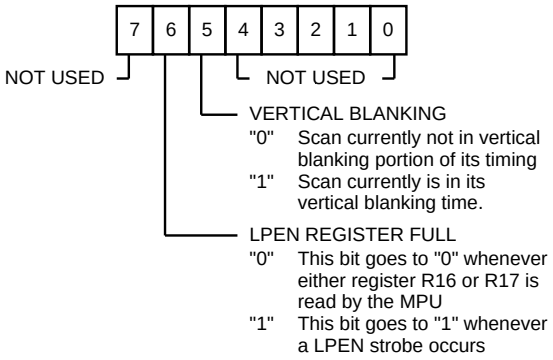
Figure 1 illustrates the format of a typical video display and is necessary to understand the functions of the various 6545-1 internal registers. Figure 2 illustrates vertical and horizontal timing. Figure 3 summarizes the internal registers and indicates their address selection and read/write capabilities.

Address Register

This is a 5-bit register which is used as a "pointer" to direct 6545-1 data transfer to and from the system MPU. Its contents is the number of the desired register (0-31). When RS is low, the this register may be loaded; when RS is high, then the register selected is the one whose identity is stored in this register.

Status Register

This register is used to monitor status of the CRTC, as follows:



Horizontal Total (R0)

This 8-bit register contains the total of displayed and non-displayed character, minus one, per horizontal line. The frequency of HSYNC is thus determined by this register.

Horizontal Displayed (R1)

This 8-bit register contains the number of displayed characters per horizontal line.

Horizontal Sync Position (R2)

This 8-bit register contains the position of the HSYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left-to-right location of the displayed text on the video screen. In this way, the side margins are adjusted.

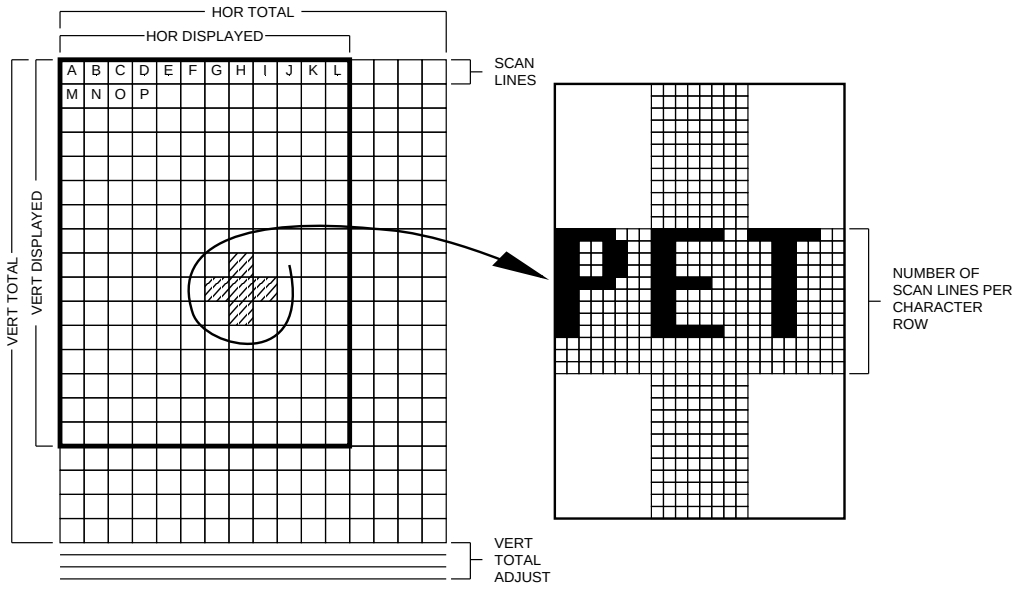


Figure 1. Video Display Format

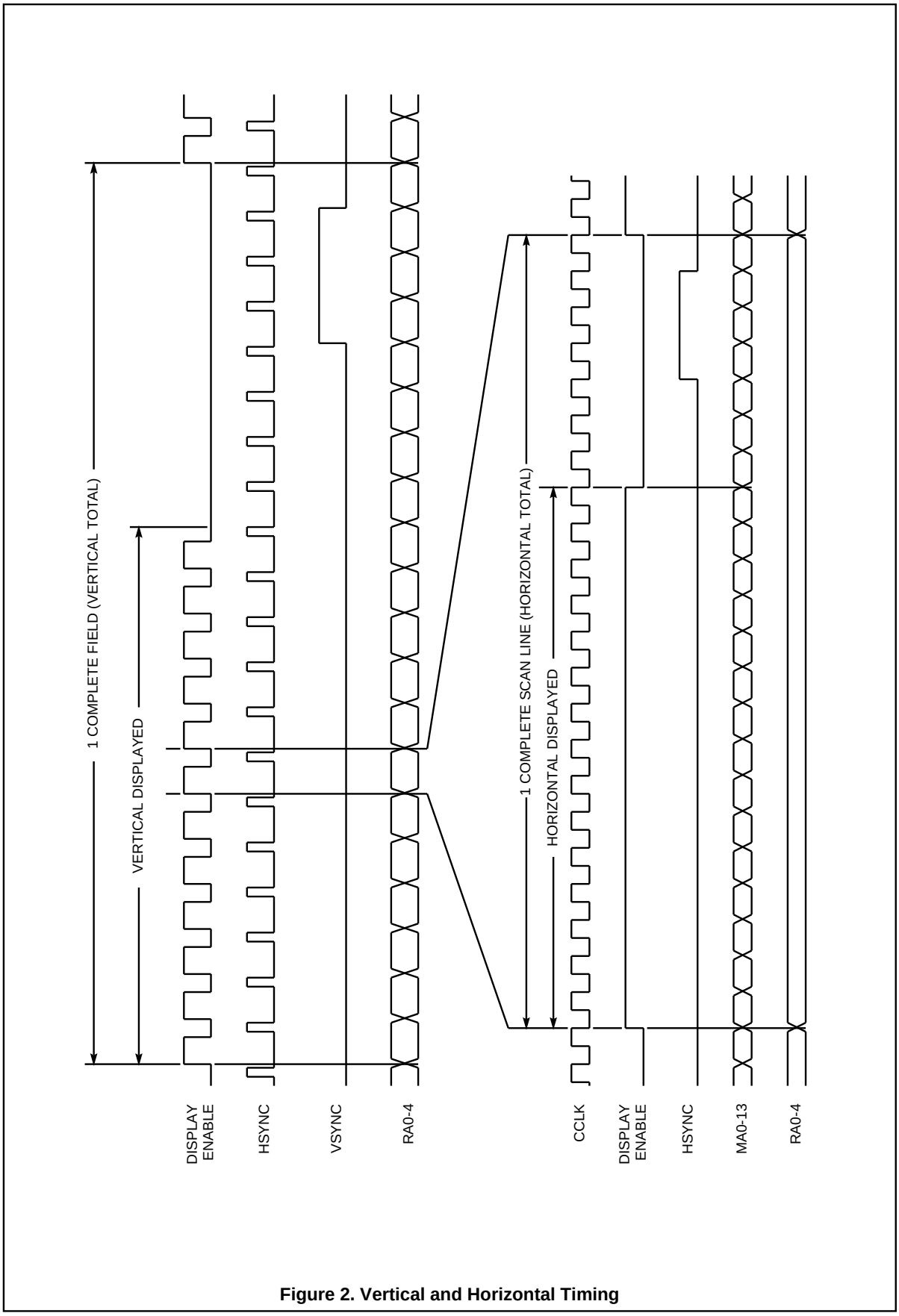
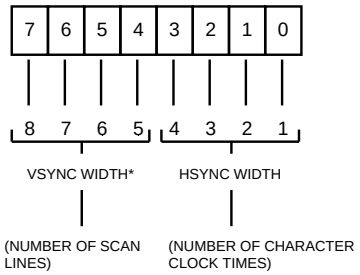


Figure 2. Vertical and Horizontal Timing

Horizontal and Vertical SYNC Widths (R3)

This 8-bit register contains the widths of both HSYNC and VSYNC, as follows:



Control of those parameters allows the 6545-1 to be interfaced to a variety of CRT monitors, since the HSYNC and VSYNC timing signals may be accommodated without the use of external one-shot timing.

Vertical Total (R4)

The Vertical Total Register is a 7-bit register containing the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency, then /RES may be used to provide absolute synchronism.

/CS	RS	Address Reg 4 3 2 1 0	Reg. No.	Register Name	Stored Info	RD	WD	Address Reg 7 6 5 4 3 2 1 0
1	-	- - - - -	-					X X X X X X X X
0	0	- - - - -	-	Address reg.	Reg. No.		yes	X X X a4 a3 a2 a1 a0
0	0	- - - - -	-	Status Reg.		yes		U L V X X X X X
0	1	0 0 0 0 0	R0	Horiz. Total	# Charac.		yes	· · · · · · · ·
0	1	0 0 0 0 1	R1	Horiz. Displayed	# Charac.		yes	· · · · · · · ·
0	1	0 0 0 1 0	R2	Horiz. Sync Position	# Charac.		yes	· · · · · · · ·
0	1	0 0 0 1 1	R3	VSYNC, HSYNC Widths	#Scan Lines & #Char. Times		yes	v3 v2 v1 v0 h3 h2 h1 h0
0	1	0 0 1 0 0	R4	Vert. Total	# Charac. Row		yes	X · · · · · · ·
0	1	0 0 1 0 1	R5	Vert. Total Adjust.	# Scan Lines		yes	X X X · · · · ·
0	1	0 0 1 1 0	R6	Vert. Displayed	# Charac. Rows		yes	X · · · · · · ·
0	1	0 0 1 1 1	R7	Vert. Sync Position	# Charac. Rows		yes	X · · · · · · ·
0	1	0 1 0 0 0	R8	Mode Control			yes	· · · · · · · ·
0	1	0 1 0 0 1	R9	Scan Line	# Scan Lines		yes	X X X · · · · ·
0	1	0 1 0 1 0	R10	Cursor Start	Scan Line No.		yes	X b1 b0 · · · · ·
0	1	0 1 0 1 1	R11	Cursor End	Scan Line No.		yes	X X X · · · · ·
0	1	0 1 1 0 0	R12	Display Start Addr (H)			yes	X X · · · · · ·
0	1	0 1 1 0 1	R13	Display Start Addr (L)			yes	· · · · · · · ·
0	1	0 1 1 1 0	R14	Cursor Position (H)		yes	yes	X X · · · · · ·
0	1	0 1 1 1 1	R15	Cursor Position (L)		yes	yes	· · · · · · · ·
0	1	1 0 0 0 0	R16	Light Pen Reg. (H)		yes		X X · · · · · ·
0	1	1 0 0 0 1	R17	Light Pen Reg. (L)		yes		· · · · · · · ·

Notes · Designates binary bit
X Designates unused bit. Reading this bit is always "0", except for R31, which does not drive the data bus at all, and for /CS "1" which operates likewise.

Figure 3. Internal Register Summary

Vertical Total Adjust (R5)

The Vertical Total Adjust Register is a 5-bit write only register containing the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

Vertical Displayed (R6)

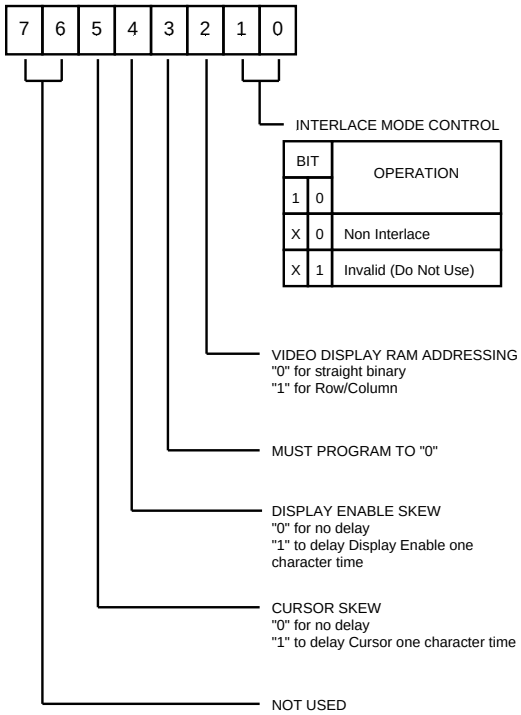
This 7-bit register contains the number of displayed character rows in each frame. In this way, the vertical size of the displayed text is determined.

Vertical Sync Position (R7)

This 7-bit register is used to select the character row time at which the VSYNC pulse is desired to occur and, thus, is used to position the displayed text in the vertical direction.

Mode Control (R8)

This register is used to select the operating modes of the 6545-1 and is outlined as follows:



Scan Line (R9)

This 5-bit register contains the number of scan lines per character row, including spacing.

Cursor Start (R10) and Cursor End (R11)

These 5-bit registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor mode, as follow:

BIT 6	BIT 5	CURSOR MODE
0	0	No Blinking
0	1	No Cursor
1	0	Blink at 1/16 field rate
1	1	Blink at 1/32 field rate

Note that the ability to program both the start and end scan line for cursor enables either block cursor or underline to be accommodated. Registers R14 and R15 are used to control the character position of the cursor over the entire 16K address field.

Display Start Address High (R12) and Low (R13)

These registers together comprise a 14-bit register whose contents is the memory address of the first character of the displayed scan (the character on the top left of the video display, as in figure 1). Subsequent memory addresses are generated by the 6545-1 as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled of changed as well via R12 and R13.

Cursor Position High (R14) and Low (R15)

These registers together comprise a 14-bit register whose contents is the memory address of the current cursor position. When the video display scan counter (MAx lines) matches the contents of this register, and when the scan line counter (RAx lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

LPEN High (R16) and Low (R17)

These registers together comprise a 14-bit register whose contents is the light pen strobe position, in terms of the video display address at which the strobe accurred. When the LPEN input changes from low to high, then, on the next negative-going edge of CCLK, the contents of the internal scan counter is stored in registers R16 and R17.

DETAILED DESCRIPTION OF OPERATION

Register Formats

Register pairs R12/R13, R14/R15 and R16/R17 are formatted in one of two ways:

1. Straight binary if register R8, bit 2 is a "0".
2. Row/Column if register R8, bit 2 is a "1". In this case the low byte is the Character Column and the high byte is the Character Row.

Figure 4 illustrates the address sequence for the video display control for each mode.

Note from Figure 4 that the straight-binary mode has the advantage that all display memory addresses are stored in a continuous memory block, starting with address 0 and ending at 1919. The disadvantage with this method is that, if it is desired to change a displayed character location, the row and column identity of the location must be converted to its binary address before the memory may be written. The Row/Column mode, on the other hand, does not need to undergo this conversion. However, memory is not used as efficiently, since the memory addresses are not continuous, but gaps exists. This requires that the system be equipped with more memory than is actually used and this extra memory is wasted. Alternatively, address compression logic may be employed to translate the Row/Column format into a continuous address block.

In this way, the user may select whichever mode is best for the given application. The trade-offs between the modes are software versus hardware. Straight-binary mode minimizes hardware requirements and Row/Column requires minimum software.

TOTAL - 90
DISPLAY - 80
TOTAL - 34
DISPLAY - 24

0	1	2	...	...	77	78	79	80	81	...	89
80	81	82	...	...	157	158	159	160	161	...	169
160	161	162	...	...	237	238	239	240	241	...	249
.							.				.
.							.				.
.							.				.
1760	1761	1762	...	...	1837	1838	1839	1840	1841	...	1849
1840	1841	1842	...	...	1917	1918	1919	1920	1921	...	1929
1920	1921	1922	...	...	1997	1998	1999	2000	2001	...	2009
2000	2001	2002	...	...	2077	2078	2079	2080	2081	...	2089
.							.				.
2640	2641	2642	...	...	2717	2718	2719	2720	2721	...	2729

STRAIGHT BINARY ADDRESSING SEQUENCE

TOTAL - 90
COLUMN ADDRESS (MA0-7)
DISPLAY - 80
TOTAL - 34
ROW ADDRESS (MA8-13)
DISPLAY - 24

0	1	2	...	...	77	78	79	80	81	...	89
256	257	258	...	...	333	334	335	336	337	...	345
512	513	514	...	...	589	590	591	592	593	...	601
.							.				.
.							.				.
.							.				.
5632	5633	5634	...	...	5709	5710	5711	5712	5713	...	5721
5888	5889	5890	...	...	5965	5966	5967	5968	5969	...	5977
6144	6145	6146	...	...	6221	6222	6223	6224	6225	...	6233
6400	6401	6402	...	...	6477	6478	6479	6480	6481	...	6489
.							.				.
8448	8449	8450	...	...	8525	8526	8527	8528	8529	...	8534

ROW/COLUMN ADDRESSING SEQUENCE

Figure 4. Display Address Sequences (with Start Address = 0) for 80 * 24 Example

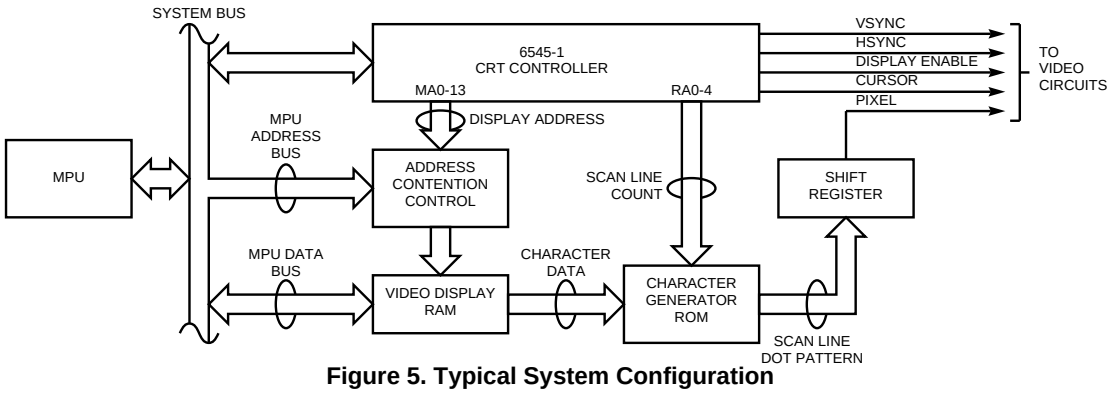


Figure 5. Typical System Configuration

Memory Contention Schemes for memory Addressing

From the diagram of Figure 4, it is clear that both the 6545-1 and the system MPU must be capable of addressing the video display memory. The 6545-1 repetitively fetches character information to generate the video signals in order to keep the screen display active. The MPU occasionally accesses the memory to change the displayed information of to read out current data characters. Three ways of resolving this dual-contention requirements are apparent:

· MPU Priority

In this technique, the address lines to the video display memory are normally driven by the 6545-1 unless the MPU needs access, in which case the MPU addresses immediately override those from the 6545-1 and the MPU has immediate access.

· Vertical Blanking

With this approach, the address circuitry is identical to the case for MPU Priority updates. The only difference is that the Vertical Retrace status bit (bit 5 of the Status Register) is used by the MPU so that access to the video display memory is only made during vertical blanking time (when bit 5 is a "1"). In this way, no visible screen perturbations result.

· phi1/phi2 Memory Interleaving

This method permits both the 6545-1 and the MPU access to the video display memory by time-sharing via the system phi1 and phi2 clocks. During the phi1 portion of each cycle (the time when phi2 is low), the 6545-1 address outputs are gated to the video display memory. In the phi2 time, the MPU address lines are switched in. In this way, both 6545-1 and the MPU have unimpeded access to the memory. Figure 6 illustrates the timings.

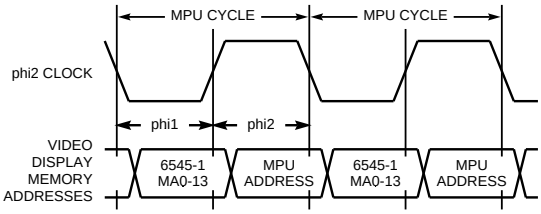


Figure 6. phi1/phi2 Interleaving

Cursor and Display Enable Skew Control

Bits 4 and 5 of the Mode Control register (R8) are used to delay the Display Enable and Cursor outputs, respectively. Figure 7 illustrates the effect of the delays.

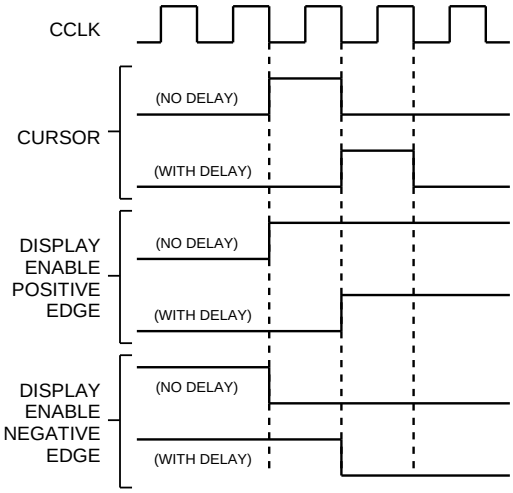


Figure 7. Cursor and Display Enable Skew

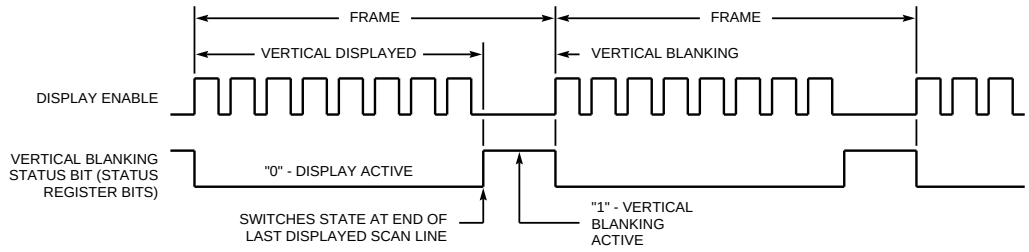


Figure 8. Operation of Vertical Blanking Status Bit

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